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2817 AF # IFW

PATENT
Attorney Docket No. 401251/TAKADA

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

ISHIDA et al.

Application No. 09/877,037

Filed: June 11, 2001

Art Unit: 2817

Examiner: S. Jones

For: MICROWAVE INTEGRATED CIRCUIT WITH CAPACITANCE VARIATION COMPENSATION

TRANSMITTAL OF
APPELLANTS' APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with 37 CFR 1.192, appellants hereby submit Appellants' Brief on Appeal in triplicate.

The items checked below are appropriate:

1. Status of Appellants

This application is on behalf of ☒ other than a small entity or ☐ a small entity.

2. Fee for Filing Brief on Appeal

Pursuant to 37 CFR 1.17(c), the fee for filing the Brief on Appeal is for: ☒ other than a small entity or ☐ a small entity.

Brief Fee Due $330.00

3. Oral Hearing

☐ Appellants request an oral hearing in accordance with 37 CFR 1.194.

4. Extension of Time

☐ Appellants petition for a one-month extension of time under 37 CFR 1.136, the fee for which is $110.00.

☒ Appellants believe that no extension of time is required. However, this conditional petition is being made to provide for the possibility that appellants have inadvertently overlooked the need for a petition and fee for extension of time.

Extension fee due with this request: $

5. Total Fee Due

The total fee due is:

Brief on Appeal Fee	$330.00
Request for Oral Hearing	$ 0.00
Extension Fee (if any)	$ 0.00

Total Fee Due: $330.00

6. Fee Payment

☐ Attached is a check in the sum of $.
☒ Charge Account No. 12-1216 the sum of $330.00. A duplicate of this transmittal is attached.

7. Fee Deficiency

☒ If any additional fee is required in connection with this communication, charge Account No. 12-1216. A duplicate copy of this transmittal is attached.

Respectfully submitted,

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Date: May 4, 2004
JAW:tps

Appeal Brief Transmittal (Revised 10/1/03)

PATENT
Attorney Docket No. 401251/TAKADA

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APPELLANTS' APPEAL BRIEF

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P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In support of the appeal from the final rejection dated January 14, 2004, Appellants now submit their Brief.

Real Party In Interest

The patent application that is the subject of this appeal is assigned to Mitsubishi Denki Kabushiki Kaisha.

Related Appeals and Interferences

There are no appeals or interferences that will directly affect or be directly affected by or have a bearing on the decision in this Appeal.

Status of Claims

This application was filed with 12 claims. In the course of prosecution, claims 13-16 were added and all of the original claims 1-12 were cancelled. Claims 13-16 remain pending. No claim is allowed and the final rejection of all claims is appealed. The claims on appeal appear on the appendix.

Status of Amendments

In response to the final rejection of January 14, 2004, the final rejection that is the subject of this Appeal, an Amendment after final rejection was filed on March 4, 2004. This amendment corrected two inadvertent errors in claim 15 but did not otherwise seek to amend any claims. According to an Advisory Action mailed March 18, 2004, this amendment was entered.

Summary of Invention

The invention concerns a monolithic microwave integrated circuit (MMIC). In the MMIC according to claim 13, a transistor has an input terminal and an input line connected to the input terminal. One electrode of a capacitor is connected to the input terminal and an open stub capacitance is connected to the input line. The open stub capacitance is connected to the input line at a position remote from the input terminal of the transistor, i.e., remote from the capacitor.

An important feature of the MMIC is an insulating film that is present at the transistor. In addition, that insulating film is the insulator of the capacitor, which is identified as an metal-insulator-metal (MIM) capacitor. The insulating film that is around the transistor affects the input capacitance of the transistor. The input capacitance of the transistor varies directly with the thickness of the insulating film, meaning that the input capacitance increases as the thickness of the film increases. As well known in the art, an MIM capacitor decreases in capacitance as the thickness of the insulating film of that capacitor increases. In the invention, these oppositely directed variations of input capacitance and of MIM capacitance with the thickness of the insulating film are exploited. An increase in one of the capacitances is compensated by the decrease in the other capacitance since each capacitance depends upon the thickness of the insulating film. In other words, since the same insulating film is employed around the transistor and also as the insulator of the MIM capacitor, if, due to processing variations, the insulating film is thicker than intended, the MIM capacitance is reduced, but the input capacitor of the transistor is increased. An insulating film that is thinner than a design thickness likewise increases the MIM capacitance while decreasing the transistor input capacitance. These changes offset each other in terms of the effective capacitance of the MMIC. Thus, the performance of the MMIC is stabilized with respect to variations in processing during the manufacture of the MMIC that result in variations in the thickness of the insulating film from a design thickness.

Figure 1 of the patent application is a schematic diagram of a circuit encompassed within the scope of claim 13. In that embodiment, the transistor 26 has an MIM capacitor 30 connected at the input terminal of the transistor. An open stub capacitance L1, indicating a length of transmission line, is connected at a line 10 to the input line 12 of the transistor 26, but at position remote from the input terminal of the transistor 26. The locations a, b, c, and d along the input line 12 indicate points of measuring the impedance of the circuit in the direction of the transistor 26. The impedances measured at each of these points are plotted on the Smith chart shown in Figure 3 of the patent application. This chart shows an impedance match at the point d is achieved through the combination of the open stub capacitance and the MIM capacitor.

Dependent claim 14 describes the MMIC as including a bias circuit connected in parallel with the MMIC capacitor. This claim encompasses the embodiment of Figure 4 of the patent application in which it can be seen that a voltage V_g is applied to a bias circuit that is connected in parallel with the MIM capacitor 30.

Claim 15 is directed to an MMIC that is analogous to the MMIC of claim 13. However, in the MMIC of claim 15, the MIM capacitor is connected to the output terminal of the transistor and the open stub capacitance is connected to the output line of the transistor at a location remote from the output terminal of the transistor. Claim 15 encompasses the embodiment of Figure 6, which is analogous to Figure 1, with the exception that the open stub capacitance and the MIM capacitor 30 are connected to the output line 12 of the transistor, rather than at the input line 12 as in Figure 1. Likewise, dependent claim 16 is analogous to dependent claim 14 in describing a bias circuit that is connected in parallel with the MIM capacitor. Claim 14 encompasses the embodiment of Figure 9 of the patent application where the bias circuit includes a second capacitor 34 and a resistor 40.

Issue

Is claim 15 anticipated by Hosoya (U.S. Patent 6,259,332)?

Grouping of Claims

All claims stand or fall together.

Argument

It is fundamental that for anticipation, a publication must disclose every element of a claim. Hosoya fails that stringent test with regard to claims 15 and 16. The assertion that Hosoya anticipates claims 15 and 16 is the basis of the rejection of claims 13 and 14. Assuming, for the sake of argument, that the secondary reference, Okada (U.S. Patent 6,628,176), stands for the proposition for which it was cited, (analogous to reverse input and output connection networks), Hosoya cannot establish *prima facie* obviousness of claims 13 and 14 because Hosoya does not anticipate claims 15 and 16. Therefore, all claims stand or fall together. Accordingly, the failure of Hosoya to anticipate claim 15 requires the reversal of both rejections.

The final rejection mailed January 14, 2004 directed attention to Figure 16 of Hosoya, a pictorial view of an MMIC. That MMIC includes a field effect transistor 1 having an output line 11 to which an MIM capacitor 18 is connected. Further, open stubs 12, 13a, and 13b are connected to that output line 11 at locations more remote from the transistor 1 than the MIM capacitor 18 that is proximate the bias pad 17.

Figure 16 of Hosoya is one of three pictorial views of MMICs in that patent. In the structure shown in Figure 16 of Hosoya, the MMIC includes a semiconductor substrate 15. Figure 17 shows a nearly identical structure except that there is a grounded metal film on the semiconductor substrate to which the source 2 of the transistor is connected. The grounded metal film surrounds and is separated from the other elements of the microwave circuit. Figure 18 is pictorial view of another similar, but not identical, circuit, which is supported on an insulating substrate 31. That insulating substrate is, in turn, mounted on a metal block 30. A review of these three pictorial views is important in understanding what element of the claimed invention that is missing from Hosoya. That missing element prevents Hosoya from anticipating or making obvious any pending claim.

As explained, in the invention, there is a single insulating film that is disposed both around the transistor, affecting its input capacitance, and that is also the insulating film of the MIM capacitor. There is no description of such a insulating film anywhere within Hosoya. Clearly, there must be an insulating film within Hosoya's MIM capacitor 18. In fact, Hosoya identifies that film as a silicon nitride film 100 microns thick (see column 11, lines 57-58 of Hosoya). In the portion of Hosoya describing the structures shown in the three pictorial views, Figures 16-18, from column 11, line 33 to column 13, line 7, Hosoya describes each of the three illustrated MMICs. The description includes identification of the compositions of the respective substrates and supporting materials, of an epitaxial resistor, of ohmic contacts, the transmission lines, and bias pads. There is no description in Hosoya in these or in the

other portions of that publication of the existence of "an insulating film around the transistor, affecting input capacitance of the transistor". Such a film is an express part of every pending claim. Further, there is no suggestion in Hosoya of such an insulating film that is also the insulating film of the MIM capacitor.

Silence is not disclosure. Therefore, when a prior art publication fails to disclose an element of a claimed invention, that publication cannot anticipate the claimed invention. With regard to Hosoya, it is plainly apparent that there is no such insulating film present around the transistor, even by implication. This conclusion is sound because Hosoya does provide extensive detail with respect to the structure of the circuits shown in the pictorial views of Figures 16-18. If such an insulating film were present it would have been described. Since there is no such film in Hosoya, a film that is an expressly claimed element in each of the four pending claims, Hosoya cannot anticipate claims 15 and 16 and cannot make obvious claim 13 and 14.

For the most fundamental of reasons, i.e., the absence of every element of the rejected claims in Hosoya, the rejection cannot be sustained as to any pending claim and must be reversed.

Respectfully submitted,

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Date: May 4, 2004
JAW/tps

APPENDIX

13. A monolithic microwave integrated circuit (MMIC) comprising:

a transistor having an input terminal and an insulating film around the transistor, affecting input capacitance of the transistor, the input capacitance changing directly with thickness of the insulating film;

an input line connected to the input terminal;

a metal-insulator-metal (MIM) capacitor, including two metal electrodes separated by part of the insulating film, one of the metal electrodes of the MIM capacitor being connected to the input terminal of the transistor; and

an open stub capacitance connected to the input line, remote from the input terminal of the transistor, capacitance of the MIM capacitor changing inversely with the thickness of the insulating film, whereby variations in the input capacitance of the transistor and the capacitance of the MIM capacitor due to variations in the thickness of the insulating film are compensated.

14. The MMIC according to claim 13 including a bias circuit connected in parallel with the MIM capacitor.

15. A monolithic microwave integrated circuit (MMIC) comprising:

a transistor having an output terminal and an insulating film around the transistor, affecting output capacitance of the transistor, the output capacitance changing directly with thickness of the insulating film;

an output line connected to the output terminal;

a metal-insulator-metal (MIM) capacitor, including two metal electrodes separated by part of the insulating film, one of the metal electrodes of the MIM capacitor being connected to the output terminal of the transistor; and

an open stub capacitance connected to the output line, remote from the output terminal of the transistor, capacitance of the MIM capacitor changing inversely with the thickness of the insulating film, whereby variations in the output capacitance of the transistor and the capacitance of the MIM capacitor due to variations in the thickness of the insulating film are compensated.

16. The MMIC according to claim 14 including a bias circuit connected in parallel with the MIM capacitor.